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Supper low noise PLL Oscillator and Low Jitter Synthesizer: Theory and Design

Han-xiong Lian

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Supper low noise PLL Oscillator and Low Jitter Synthesizer: Theory and Design Han-xiong Lian Nowaday, the supper low noise PLL oscillator and the supper low jitter synthesizer have been used in the worldwide communications system. Where, the former is used for the satellite communications and the latter is used for the cellular phone. The main idea to obtain a supper low noise PLL oscillator is to use a high Q resonator, such as the dielectric resonator, with a suitable phase-locked loop. To design a supper low jitter synthesizer, the best way is to set up a solid background about the synthesizer, which includes: The analogy PLL oscillator (linear analysis and nonlinear analysis), The digital PLL oscillator, using the symbol analysis and the analog PLL analysis, The synthesizer, using the symbol analysis and the sample PLL analysis. Mean while, the digital-hybrid PLL can be used for the 10 Gbit/s data recovery in the 10 Gbit/s optical fiber transponder. This book will provide you all of those information. Meanwhile, provider you the design formulas, design examples and the final schematics. The author have been involved in the design and development of all of those projects above for almost 30 years. Therefore, this book is very clear not only in theoretical analysis but also in experimental.

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